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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,122	02/11/2004	Taiji Noda	60188-766	2607

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EXAMINER	
LEE, CHEUNG	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 01/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,122	NODA, TAIJI	
	Examiner	Art Unit	
	Cheung Lee	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,16 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,16 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11-09-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Notice to Applicant

1. Applicant's Amendments and Response to the Office Action mailed on August 9, 2005 have been entered and made of record.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on November 9, 2005 was filed after the first action on the merits. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Amendment

3. In view of Applicant's Amendments and arguments filed on November 9, 2005, the rejections of claims 1-14 under 35 U.S.C. 103(a) have been withdrawn. Applicant's arguments have been rendered moot in view of the new ground of rejection given below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-14 and 16-17 are rejected under 35 U.S.C. 103(a) as being obvious over Noda et al. (U.S. Patent 6,432,802; hereinafter "Noda") in view of Khosla et al. (U.S. Patent 5966623; hereinafter "Khosla").

2. With respect to claim 1, Noda discloses a fabrication method for a semiconductor device comprising the steps of: (a) forming a gate electrode (col. 6, lines 55-59; fig. 1(b), item 102) on a semiconductor region of a first conductivity type (col. 6, lines 41-54) with a gate insulating film interposed therebetween (col. 6 lines 55-59; fig. 1(b), item 101); (b) forming extension implanted layers in the semiconductor region by implanting first impurities of a second conductivity type in the semiconductor region using the gate electrode as a mask (col. 6, lines 60-67 and col. 7, lines 1-4); and (d), forming extension diffused layers of the second conductivity type made from diffusion of the first impurities in top portions of the semiconductor region (fig. 2(a), item 105) by performing first heat treatment (col. 7, lines 16-37). However, Noda does not disclose expressly a step (c), after the step (b), forming fluorine implanted layers in upper portions of the extension implanted layers by implanting fluorine in the semiconductor region using the gate electrode as a mask.

Khosla discloses implantation of fluorine into silicon wafers (col. 4, lines 45-61). Also, Khosla discloses that the presence of fluorine reduces boron diffusion (col. 3, line 60-col. 4, line 2).

The examiner takes the position that it is obvious to use the gate electrode as a mask during the fluorine implantation since Noda uses the gate electrode as a mask during the first implantation (col. 6, lines 60-67). And it is obvious to implant fluorine in

upper portions of the extension implanted layers to reduce diffusion of the first impurities.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a fluorine implanted layer in the semiconductor region, as taught by Khosla. The motivation for doing so would have been to achieve reduction of the effects of dopant channeling and diffusion of the impurities.

3. With respect to claim 2, Noda discloses a fabrication method for a semiconductor device as set forth in claim 1, but Noda does not disclose expressly the dose of fluorine in the step (c) is not less than $1x10^{13}/cm^2$ and also in the level at which the semiconductor region is kept from becoming amorphous.

Khosla discloses the fluorine implantation as described in claim 1, and also discloses the preferable fluorine dose, which ranges from $1x10^{13}$ cm^{-2} to $1x10^{15}$ cm^{-2} (col. 5, lines 7-25). At least at the lower range of the dose of fluorine is in the level at which the semiconductor region is kept from becoming amorphous.

4. With respect to claim 3, Noda discloses a fabrication method for a semiconductor device as set forth in claim 1, but Noda does not disclose expressly the dose of fluorine in the step (c) is less than $3x10^{14}/cm^2$.

Khosla discloses the preferable dose of fluorine, which ranges from $1x10^{13}$ cm^{-2} to $1x10^{15}$ cm^{-2} (col. 5, lines 7-25). Therefore, this claim limitation is met whenever the dose of fluorine is between $1x10^{13}$ cm^{-2} and $3x10^{14}$ cm^{-2}.

5. With respect to claim 4, Noda discloses a fabrication method for a semiconductor device as set forth in claim 1, wherein the implantation projected range of fluorine in the

step (c) is roughly the same as the implantation projected range of the first impurities in the step (b). Noda discloses the p-type and n-type dopant doses (col. 6, lines 60-67 and col. 7, lines 1-4), which are within the fluorine dose range as set forth in claim 3.

6. With respect to claim 5, Noda discloses a fabrication method for a semiconductor device as set forth in claim 1, wherein the step (b) includes the step of forming pocket implanted layers in the semiconductor region (fig. 1(c), item 106A) by implanting second impurities of the first conductivity type in the semiconductor region (col. 7, lines 5-15) using the gate electrode as a mask, and in the step (d), pocket diffused layers of the first conductivity type made from diffusion of the second impurities (fig. 2(a), item 106) are formed in portions of the semiconductor region under the extension diffused layers (fig. 2(a), item 105) by performing the first heat treatment (col. 7, lines 16-37).

7. With respect to claim 6, Noda discloses a fabrication method for a semiconductor device as set forth in claim 1, wherein after the step (d), the method further comprises the steps of: (e) forming sidewalls (fig. 2(b), item 107) made of an insulating film on walls of the gate electrode (col. 7, lines 37-44); (f) forming source/drain implanted layers in the semiconductor region by implanting third impurities of the second conductivity type in the semiconductor region using the gate electrode and the sidewalls as a mask (col. 7, lines 45-58); and (g) after the step (f), forming source/drain diffused layers of the second conductivity type made from diffusion of the third impurities (fig. 2(c), item 104) in portions of the semiconductor region on the outer sides of the sidewall (col. 7, lines 45-58).

8. With respect to claim 7, Noda discloses a fabrication method for a semiconductor device as set forth in claim 1, wherein in the step (d), the fluorine in the fluorine implanted layers diffuses while interacting with point defects, so that excessive point defects induced in the semiconductor region are removed.

According to Noda, the transient enhanced diffusion (hereinafter "TED") is a phenomenon causes by point defects, existing in excessive numbers between lattice sites (col. 2, lines 29-36). Khosla discloses that fluorination can be used to neutralize the transition metal impurities (col. 3, lines 29-38). And thermal treatments at appropriate temperatures are used to initiate the interdiffusion and reaction between fluorine and metal contaminants, thus reducing the number of mid-gap impurities (col. 3, lines 29-38). Therefore, the examiner takes the position that it is obvious that the step of fluorine diffusion exists to remove the excessive point defects induced in the semiconductor region.

9. With respect to claim 8, Noda discloses a fabrication method for a semiconductor device as set forth in claim 1, further comprising the step of: performing extremely low temperature heat treatment for the semiconductor region before the step (d) and after the step (c), to recover crystal damage produced in the semiconductor region due to the implantation of the first impurities (col. 7, lines 16-37; col. 8, lines 25-30) and the fluorine without substantially allowing diffusion of the first impurities in the extension implanted layers.

According to Khosla, fluorine implanted layer is heat treated to annihilate ion induced crystalline damage (col. 5, lines 55-67). Also, according to Noda, another

annealing process is conducted with an elevated temperature after low temperature heat treatment, and this heat treatment is carried out to form the dopant diffused layers (col. 8, lines 25-33). So, the examiner takes the position that it would have been obvious that the step of extremely low temperature heat treatment is performed without substantially allowing diffusion of the first impurities.

10. With respect to claim 9, Noda does not disclose wherein the extremely low temperature heat treatment has a heating temperature of 400° C to 600° C. However, Noda discloses a very low temperature annealing process between 400° C and 550° C (col. 7, lines 16-21). In the case where claimed ranges "overlap or lie inside rages disclosed by the prior art" a prima facie case of obviousness exists. *In re Wertheim*, 541 F. 2d 257, 191 USPQ 90 (CCPA 1976); *In re Woodruff*, 919 F. 2d 1575, 16 USPQ 2d 1934 (Fed. Cir. 1990).

11. With respect to claim 10, Noda discloses a fabrication method for a semiconductor device as set forth in claim 1, wherein the first heat treatment in the step (d) is rapid thermal annealing in which the temperature rise rate is about 100° C/s or more (col. 7, lines 20-30), the heating temperature is about 850° C to 1050° C (col. 7, lines 20-30), and the peak temperature is held for about ten seconds at the longest or is not held at all (col. 7, lines 20-30), however, Noda does not disclose expressly that the temperature drop rate is about 80° C/s or more.

Similar to the claimed invention, Noda discloses the heat treatment is carried out to form the extended high-concentration dopant diffused layer and pocket dopant diffused layer with similar heating temperature range and temperature rise rate (col. 8,

lines 25-33), so the examiner takes the position that it would have been obvious that the temperature drop rate would be about 80° C/s.

12. With respect to claim 11, Noda discloses a fabrication method for a semiconductor device as set forth in claim 1, wherein the first impurities in the step (b) are boron or indium (col. 6, lines 60-67; col. 8, line 25).

13. With respect to claim 12, Noda discloses a fabrication method for a semiconductor device as set forth in claim 1, wherein the first impurities in the step (b) are arsenic (col. 7, lines 1-4; col. 8, line 25).

14. With respect to claim 13, Noda discloses a fabrication method for a semiconductor device as set forth in claim 12, but Noda does not disclose expressly wherein during the first heat treatment in the step (d), the first impurities in the extension implanted layers diffuse in a state in which the fluorine has captured atomic vacancies produced in top portions of the semiconductor region.

The fluorine implantation in Khosla causes same results as the claimed steps of fluorine capturing atomic vacancies produced in top portions of the semiconductor region during the first impurities in the extension layer diffusion. The fluorine implantation reduces or neutralizes the transition or diffusion of metal impurities (col. 3, line 25-col. 4, line 2). Therefore, the examiner takes the position that the fluorine implantation process taught by Khosla inherently performs the step of capturing atomic vacancies in top of the semiconductor region.

15. With respect to claim 14, Noda discloses a fabrication method for a semiconductor device as set forth in claim 1, wherein the dose for the implantation of

the first impurities in the step (b) is in a level at which the semiconductor region is kept from becoming amorphous (col. 5, lines 29-42), and the extension diffused layers having a predetermined impurity concentration are formed by repeating a series of process steps composed of implanting the first impurities in the step (b) (col. 15, lines 33-45), and performing the first heat treatment in the step (d) (col. 15, lines 33-45).

Noda does not disclose expressly the fluorine implantation step. However, Khosla discloses fluorine implantation (col. 4, lines 45-61). So, the examiner takes the position that it would have been obvious that in the combined teaching of Noda and Khosla the steps to form the extension diffused layers having predetermined impurity concentration by repeating step (b), (c), and (d) are performed.

16. With respect to claim 16, Noda in view of Khosla does not disclose expressly wherein the dose of fluorine in the step (c) is not less than $1x10^{13}/cm^2$ and less than $3x10^{14}/cm^2$. However, Khosla discloses the preferable fluorine dose, which ranges from $1x10^{13}$ cm^{-2} to $1x10^{15}$ cm^{-2} (col. 5, lines 7-25). In the case where claimed ranges "overlap or lie inside rages disclosed by the prior art" a prima facie case of obviousness exists. *In re Wertheim*, 541 F. 2d 257, 191 USPQ 90 (CCPA 1976); *In re Woodruff*, 919 F. 2d 1575, 16 USPQ 2d 1934 (Fed. Cir. 1990).

17. With respect to claim 17, Noda in view of Khosla does not disclose expressly wherein in the step (c), even when fluorine is implanted the semiconductor region is kept from becoming amorphous. However, Khosla discloses the preferable fluorine dose, which ranges from $1x10^{13}$ cm^{-2} to $1x10^{15}$ cm^{-2} (col. 5, lines 7-25). And at least at

the lower range of the dose of fluorine is in the level at which the semiconductor region is kept from becoming amorphous.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cheung Lee whose telephone number is 571-272-5977. The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cheung Lee

January 17, 2006

HA NGUYEN
PRIMARY EXAMINER